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(54) Configurable logic array.

(57) A special interconnect circuit which connects adjacent configurable logic elements (CLEs) in a configurable logic array (CLA) without using the general interconnect structure of the CLA. In one embodiment, an array of CLEs is arranged in rows and columns and a special vertical lead circuit is provided which connects an output lead of a given CLE in a given column to a selected input lead of the CLE above it and below in the same column. Special horizontal lead circuits are provided which connect a given output lead of a given CLE to a selected adjacent input lead of the CLE in the same row.

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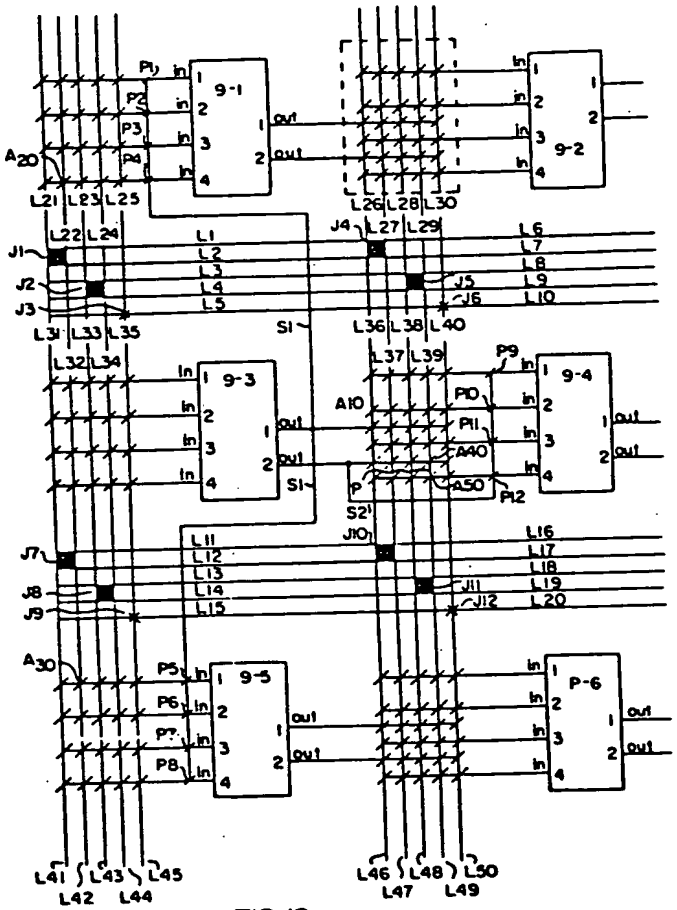
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L38
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L43
L44
L45
L46
L47
L48
L49
L50
in
out

FIG 10

CONFIGURABLE LOGIC ARRAY

DESCRIPTION

This invention relates to a configurable logic array.

As explained in detail later, a configurable logic element (CLE) also referred to herein as a logic element, is a combination of devices which are capable of being electrically interconnected by switches operated in response to control bits to form any one of a plurality of logical functions.

Each CLE can include all the circuit elements necessary to provide one or more of the functions provided by an AND gate, flip flop, latch, inverter, NOR gate, exclusive OR gate, and combinations of these functions to form more complex functions. The particular function to be carried out by a CLE is determined by control signals applied to the CLE from control logic. Depending on the control signals, the CLE can function as an AND gate, an OR gate, a NOR gate, a NAND gate or an exclusive OR gate or any one of a number of other logic elements without any change in physical structure. The control logic stores and generates control signals which control the configuration of each CLE.

The control logic is typically formed integrally with and as part of the integrated circuit chip containing the CLE. However, if desired the control information can be stored and/or generated outside this integrated circuit and transmitted through pins to the CLE.

In general, a given set of control signals is transmitted to one CLE to control the configuration of that CLE. The control logic is thus arranged to provide any one set of a plurality of sets of control bits to each CLE on the chip. The actual set of control bits provided to each CLE integrated circuit chip depends on the function to be carried out by the integrated

circuit chip or by each CLE on the chip. The configuration of each CLE on the chip is determined by the intended function of the total chip and by the intended formation of that CLE as part of the chip.

A configurable logic array (CLA) comprises a plurality of CLEs, each having one or more input leads and one or more output leads, a set of access functions for each input lead and for each output lead, and a general interconnect structure. The general interconnect structure comprises a plurality of general interconnect leads and a plurality of general interconnect junctions. The general interconnect structure has the property that for each lead in the general interconnect structure, there is a programming of the general interconnect junctions which connects the given general interconnect leads to one or more other general interconnect leads by means of a general interconnect junction. An access junction is a programmable junction for connecting a general interconnect lead to an input lead of a CLE or for connecting an output lead of the CLE to a general interconnect lead.

A CLA has the property that there is always a programming of the junctions (both access and general interconnect) so that a given output lead of a given CLE within the CLA can be connected to a given input lead of any other CLE within the CLA.

The junctions in the general interconnect structure and the access junctions are programmed by control signals generated by the control logic described above. A selection of control signals to configure each CLE in a CLA together with a selection of control signals to configure the access functions and the junctions of the general interconnect structure results in one configuration of the CLA.

This invention accordingly provides special

interconnect circuitry which connects selected CLEs in a CLA without using the general interconnect structure. The invention can thus provide on-chip special programmable interconnection circuits between selected adjacent configurable logic elements in a configurable logic array (CLA). In one embodiment for a CLA containing at least a first, a second, a third and a fourth CLE, a special interconnection circuit is provided which permits an output signal on a first output lead of the second CLE to be connected to a selected input lead of the first and third CLE and permits an output signal on a second output lead of the second CLE to be connected to a selected input lead in the fourth CLE. Typically the first and third CLE are in the same column as the second CLE and the fourth CLE is in the same row as the second CLE.

The use of the special interconnect circuits of the invention reduces the use of the general interconnect structure. The reduction in the utilization of the general interconnect structures is so substantial that in many embodiments the number of general interconnect leads and the number of general interconnect junctions is reduced, thus reducing die size.

Frequently, when interconnecting logic elements in a configurable logic array, the access junctions and the junctions of the general interconnect structure are programmed so that the output of one logic element is connected to only one or two other logic elements. If the logic elements that are interconnected are physically close together (and they typically will be placed that way to facilitate interconnecting), the present invention allows a significant amount of general interconnect structure to be eliminated, that is, the special interconnect so reduces the utilization of the general interconnect structure that the overall amount of general interconnect structure provided may be reduced,

thus reducing die size. Also, the speed of signals through this special interconnect will be improved since the number of junctions and the amount of capacitance on the path will be reduced. This type of interconnect is particularly useful when implementing MSI type functions, e.g., shift registers and counters, where adjacent logic elements must be interconnected.

This invention is further described below, by way of illustration, with reference to the accompanying drawings, in which:

Figure 1 illustrates some of the various logic functions capable of being implemented in each logic element in a configurable logic array;

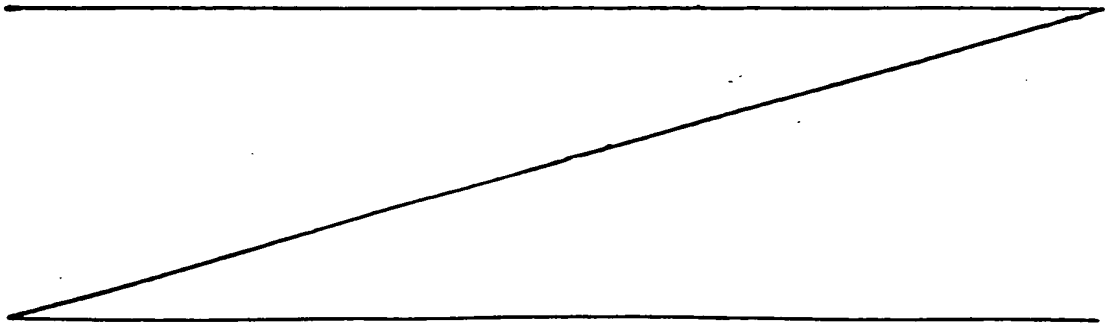
Figure 2 illustrates the internal logic structure of one possible configurable logic element capable of implementing a number of useful functions of two variables A and B;

Figure 3A illustrates a 16 bit RAM circuit wherein any one of sixteen possible input states is capable of being identified and 2^{16} functions are capable of being implemented;

Figure 3B illustrates a selection structure for selecting any one of sixteen bits capable of implementing 2^{16} functions, for transmittal to an output lead;

Figure 3C illustrates one possible Karnaugh map for the structure of Figure 3A;

Figure 3D illustrates the logic gates represented by placing a binary one in the Karnaugh map of Figure 3C at



the intersections of the first and second rows and the first column.

Figure 4A illustrates a plurality of configurable logic elements (shown as nine logic elements) formed on an integrated circuit chip together with programmable interconnects formed between selected leads to yield desired logic functions and with selected input/output pads and interconnections of the leads between logic elements;

Figure 4B shows the key to the cross-connections between crossing conductive leads in Figure 4A;

Figure 5 represents a portion of the circuitry of a novel combination static and dynamic shift register appropriate for use with the configurable logic array of this invention;

Figures 6A through 6H represent wave forms of use in explaining the operation of the structure of Figure 5;

Figure 7A represents a schematic diagram of a configurable logic array showing nine of N configurable logic elements where N is a selected integer greater than 9 and selected interconnections between conductive leads;

Figures 7B-1 through 7B-7 form the key showing the types of interconnections made by the symbols shown in Figure 7A;

Figures 8A through 8G illustrate various topologies for forming interconnections between two or more leads of a configurable logic array;

Figure 9 shows a configurable logic array without the special interconnect circuit of this invention;

Figure 10 shows the configurable logic array of Figure 9 with the special interconnect circuit of this invention; and

Figure 11 lists the pass transistor connecting lead A with lead B in Figure 8B.

U.S. Application No. 588,478, filed 12 March 1984, on an invention of Ross H. Freeman entitled "Configurable Logic Array" is incorporated herein by reference.

It is necessary to explain the configurable logic elements and general interconnect structure of the configurable logic array described in the above copending application in order to explain the special interconnect structure of the present invention.

Figure 1 illustrates certain logic functions capable of being implemented by a configurable logic element. The 28 functions shown in Figure 1 are merely illustrative and other elements not shown can, if desired, be implemented by a configurable logic element. The following functions are shown:

Element	Function
1	AND gate
2	NAND gate
3	AND gate with inverted input
4	NAND gate with inverted input
5	OR gate
6	NOR gate
7	exclusive OR gate
8	exclusive NOR gate
9	3 input AND gate
10	3 input NAND gate
11	3 input OR gate
12	3 input NOR gate
13	OR gate with one input comprising AND gate
14	NOR gate with one input comprising AND gate
15	AND gate with one input comprising OR gate
16	NAND gate with one input comprising OR gate
17	3 input AND gate with one input inverted

18	3 input NAND gate with one inverted input
19	3 input OR gate with one inverted input
20	3 lead NOR gate with one inverted input
21	one of two inputs multiplexer
22	inverting one of two inputs multiplexer
23	"D" flip flop with reset
24	Set-Reset latch
25	"D" flip-flop with reset and inverted output
26	Set-reset latch with reset and inverted output
27	"D" flip-flop with set
28	"D" flip-flop with set and inverted output

Of course, other logic functions can also be implemented in a configurable logic element.

Figure 2 illustrates the internal logic structure of one possible configurable logic element which is capable of implementing all useful basic functions of the two variables A and B, with the functions being selected by configuration control signals C0, $\bar{C}\bar{0}$, C1, $\bar{C}\bar{1}$, ... through C5 on control leads CO, $\bar{C}\bar{0}$, ... through C5. In this example each control lead is connected to the gate of an N channel enhancement mode pass transistor. To implement an AND gate function using the structure shown in Figure 2, the input leads labeled A and B are shunted past inverters 21 and 22, respectively, to AND gate 25 by high level signals on the C1 and C0 configuration control leads which, being connected to the gates of N channel enhancement mode pass transistors 29c and 29d, cause pass transistors 29c and 29d to turn on.

Low level signals are applied to the configuration control leads $\bar{C}\bar{0}$ and $\bar{C}\bar{1}$, thus blocking the output signals of inverters 21 and 22 from AND gate 25. In addition, a high level signal on lead C5 is applied to enable AND gate 25. Thus three input AND gate 25 functions as a two-input AND gate with respect to the signals A and B.

The output signal of AND gate 25 provides one input signal to NOR gate 26. A second input signal to NOR gate 26 is provided by the output signal of AND gate 24. The output signal of AND gate 24 is held at a logical 0 by applying a logical 0 to configuration control lead C4. Thus the control signals C2 and C3 are "don't cares", that is, these signals can be high or low without affecting the output signal of AND gate 24. Since the output signal of AND gate 24 is a logical 0, and since the tristate control input signal to NOR gate 26 is a logical 0, it is easy to see that AND gate 25, AND gate 24 and NOR gate 26 function together as a NAND gate with respect to input signals A and B. Since the tri-state control signal input to NOR gate 27 is a logical 0 (except during reset), NOR gate 27 serves as an inverter with respect to the output signal of NOR gate 26. The output signal of NOR gate 26 is applied to the gate of N channel transistor 29a (the source of which is grounded and the drain of which is connected to output lead 2) and the complement of the output signal of NOR gate 26 is applied to the gate of N channel transistor 29b (the source of which is connected to a power supply and the drain of which is connected to both the output lead 28 and the drain of N channel transistor 29a). Thus, transistors 29a and 29b function as an inverter with respect to the output signal of NOR gate 26. Thus, the structure of Figure 2 configured as described above performs the function of an AND gate with respect to the signals A and B. Other logic functions can also be produced by appropriate selection of the control signals to be supplied to the configuration control leads C0 through C5 to activate the appropriate pass transistors and gates within the structure.

Figure 3A illustrates a 16 bit RAM capable of producing an output signal in response to any one of sixteen possible combinations of input signals. Thus input signals A and B control the X decoder to select any one

of the four columns in the 16 bit RAM. Input signals C and D control the Y decoder to select any one of the four rows in the 16 bit RAM. The 16 bit RAM produces an output signal representative of the bit at the intersection of the selected row and column. There are 16 such intersections and thus sixteen such bits. There are 2^{16} possible combinations of functions capable of being represented by 16 bits. Thus, if a NOR gate is to be simulated by the 16 bits in the RAM, the Karnough map for the RAM would be as shown in Figure 3C. In Figure 3C all bits are "0" except the bit at the intersection of the first row (representing A=0, B=0) and the first column (representing C=0, D=0). Should a less frequently used function be desired to be generated by the 16 bit RAM, (for example, should a "1" output signal be desired for A=1, B=0, C=0 and D=0) then a binary "1" is stored at the intersection of the second row and the first column. Should a binary "1" be desired both when A=0, B=0, C=0 and D=0 and also when A=1, B=0, C=0 and D=0, then a binary "1" is stored at each of the intersections of the first column with the first row and the second row. The logic circuit represented by this loading of the RAM is as shown in Figure 3D. Thus the RAM of Figure 3A represents an elegant and simple implementation of any one of 2^{16} logic functions.

Figure 3B shows another structure for yielding any one of sixteen select bits. Each of registers 0-15 in the vertical column to the left labeled "16 Select Bits", contains a selected signal, either a binary 1 or 0. By selecting the proper combination of A, B, C, and D, a particular bit stored in a particular one of the sixteen locations in the 16 Select Bits register is transmitted to the output lead. Thus, for example, to transmit the bit in the "1" register to the output lead, the signal A, B, C, D is applied to the leads so labeled. To transmit the signal labeled "15" in the sixteenth location in the 16 Select Bits register to the output lead, the signal A,

$\bar{B}$, $\bar{C}$, and $\bar{D}$ is applied to the appropriate columns. Again, any one of 2^{16} logic functions can be implemented using this structure.

Figures 4A illustrates a configurable logic array containing nine configurable logical elements. As shown in Figure 4a, each CLE of the nine CLEs 40-1 through 40-9 has a plurality of input leads and one or more output leads. Each input lead has a plurality of access junctions each connecting a selected general interconnect lead to the input lead. The access junctions for input lead 2 of CLE 40-7 are labeled A1 through A4 in Figure 4a. The access junctions for the other input leads are indicated schematically but are not labeled for the sake of clarity. Similarly, each output lead of each CLE has a plurality of access junctions each connecting the output lead to a corresponding one of the general interconnect leads. The access junctions are indicated schematically for each output lead of each CLE in Figure 4a. The access junctions for the output lead of CLE 40-7 are labeled B1 through B5. The leads in Figure 4a which are neither input leads nor output leads are called general interconnect leads and the junctions in Figure 4a which are not access junctions for input and output leads are called general interconnect junctions. As shown in Figure 4A, nine logic elements are placed on an integrated circuit chip together with programmable access junctions and a general interconnect structure which comprises general interconnect leads and programmable general interconnect junctions for connecting various leads to other leads. The general interconnect structure set of general interconnect leads and of programmable junctions interconnecting the general interconnect leads have the property that for each general interconnect lead in the general interconnect structure there is a programming of the general interconnect junctions which connects the given general interconnect lead to one or more other leads in the general interconnect structure. Moreover, there is a programming of the

junctions (both access and general interconnect) such that for any given output lead of any CLE in the CLA, and for any given input lead of any other CLE in the CLA, there is a programming of the junctions such that the given output lead is connected to the given input lead. An electrical path from a given output lead to a given input lead always contains at least two access junctions and at least a portion of a general interconnect lead. For example, one electrical path from the output lead of CLE 40-8 to the second input lead of CLE 40-9 contains access junctions A7 and B7 and the marked portion P of a general interconnect lead. Typically, an electrical path from an output lead of one CLE to an input lead of another CLE will also contain one or more general interconnect junctions. Each of logic elements 40-1 through 40-9 represents a collection of circuitry such as that shown in Figure 2 or some similar structure capable of being configured as described above in Figure 2 to perform any one of a number of logic functions. To program the circuitry, (both the configurable interconnect switches and the configurable logic elments), selected signals are applied to input leads identified as configuration control input leads thereby to generate a desired logical function in each of the logic elements and to interconnect the logic elements as desired. In Figure 4A, no specific lead has been identified as an input lead for the configuration control signals. However, any particular I/O pad can be selected for this purpose. The configuration control bits can be input into the configurable logic array either in series or in parallel depending upon design considerations where they are typically stored in a programming register (not shown). Alternatively, the configuration control bits may be stored in a memory on chip. In addition, another I/O pad will be used on input clock signals which are used, inter alia, for the loading of the configuration control signals into the programming register. When the configurable logic array shown in

Figure 4A has been configured, selected output signals of logic elements 40-1 through 40-9 are provided to selected I/O pads. Figure 4B illustrates the meaning of the junction symbols used in Figure 4A.

To configure a logic element such as logic element 40-1 (Figure 4A, 4B) a number of bits must be applied to the configuration control leads such as leads C0 through C5, as shown, for example, in Figure 2. To do this, a shift register, for example, is utilized as part of each configurable logic element. Figure 5 illustrates a shift register which may be used. The shift register of Figure 5 is illustrated showing two basic storage cells. Each storage cell is capable of storing one bit of information. Of course, an actual shift register will contain as many storage cells as required to configure the logic element of which the shift register is a part, to its desired configuration. In operation, an input signal is applied to input lead 58. This input signal (shown in Figure 6D) contains bit stream to be stored in the shift register as configuration control bits to configure the configurable logic element to perform a desired logic function or to configure (program) an access junction or a general interconnect junction between general interconnect leads in a manner to be described shortly. Thus the sequence of pulses applied to input lead 58 represents those pulses which when stored in the storage cells of the shift register will activate the configuration control bits in the proper manner to achieve the desired functional and/or interconnection result. For example, if the circuit of Figure 2 is to be configured to form an AND gate, the pulses C0, C1, C2, C3, C4, and C5 would be represented by 1,1,X,X, 0,1.

The sequence of pulses applied to input lead 58 is synchronized with clocking pulses $\Phi 1$ and $\Phi 2$ applied to leads 57 and 59 respectively. Thus in the first period of operation clocking pulse $\Phi 1$ goes high (Fig. 6A), clocking pulse $\Phi 2$ is low (Fig. 6B), the hold signal

(Fig. 6C) is low during shifting thereby facilitating the passage of data through sequentially connected cells 5-1, 5-2 et al. of the shift register. To shift the pattern 01010 into the shift register, the following operations occur: The input signal on lead 58 is low during approximately the first half cycle of the clocking period t1. The output signal $\bar{Q}\bar{1}$ of inverter 51-1 goes to a high level in response to the low level input signal and $\Phi 1$ high to enable pass transistor 53-1. Some time through the first clocking period t1, the clock signal $\Phi 1$ goes low (Fig. 6A) and the clock signal $\Phi 2$ shortly thereafter goes high (Fig. 6B) to enable pass transistor 55-1. Consequently, the high level output signal $\bar{Q}\bar{1}$ is transmitted to the input lead of inverter 52-1 by enabled pass transistor 55-1 and thereby produces a low level output signal Q1 on the output lead of inverter 52-1. Thus at the end of period t1, the output signal Q1 (Figure 6F) from inverter 52-1 is low level. The output signals $\bar{Q}\bar{2}$ and Q2 from inverters 51-2 and 52-2 in the second cell are still indeterminate because no known signal has yet propagated to the second storage cell 5-2 to change the signals of these inverters to a known state.

At the beginning of the second period (labeled "t2" in Fig. 6A), $\Phi 1$ goes high (Fig. 6A) and $\Phi 2$ is low (Fig. 6B) having gone low before period t1 ended. The input signal (Figure 6D) now has risen to a high level representing a binary 1 and thus the output signal $\bar{Q}\bar{1}$ of inverter 51-1 has gone low. The output signal Q1 of inverter 52-1 remains low because pass transistor 55-1 is held off by the low level $\Phi 2$ signal. Some time through the second period $\Phi 1$ goes low followed a fraction of time later by $\Phi 2$ going high. At this time, the output signal $\bar{Q}\bar{1}$ is transmitted through pass transistor 55-1 to inverter 52-1 thereby driving the output signal Q1 from inverter 52-1 to high level. Meanwhile, during period t2 the previous low level signal on Q1 has driven the output signal $\bar{Q}\bar{2}$ of inverter 51-2 to a high level when Q1 was at

a high level to enable pass transistor 53-2 and the change in Φ2 from a low level to a high level in the second half of period t2 to enable pass transistor 55-2 drives the output signal Q2 from inverter 52-2 to a low level. In this manner, the input signal on lead 58 (Fig. 6D) is transmitted through each of the cells 5-1, 5-2, 5-3 et al. in the shift register. Upon the transfer into the shift register of the desired information, the hold signal (Figure 6C) is enabled (i.e., driven to a high level) thereby to connect the feedback leads 50-1, 50-2, and 50-3 et al. from the output leads of inverters 52 to the input leads of inverters 51 so as to hold the information then in each cell indefinitely. In operation, the signal stored in a given cell, e.g. 5-1, is connected to a configuration control or to an interconnect pass device.

The $\bar{Q}_1$, Q_1, $\bar{Q}_1$, Q_2, etc., of the shift register are directly connected to the (configuration) control inputs of a logic element or the pass devices of the general interconnect junctions.

When Φ1 is low, Φ2 and hold may be brought high, thus holding the data indefinitely. The entire shift register may be set or cleared by setting or clearing the input with Φ1 and Φ2 both high and HOLD low. Enough set/reset time must be allowed for the signal to propagate the entire length of the shift register to clear the shift register in this manner. Naturally this time is dependent upon the length of the shift register.

The shift register operates in its dynamic phase by storing the information being shifted as charge on the gates of the transistors (not shown in Figure 5 but well-known) comprising inventers 51-1, 52-1, 51-2, 52-2 et al. of the shift register. These inverters are of well-known design and will not be described in detail. The use of dynamic shift register is important because a dynamic shift register uses six transistors and thus

takes up very little area. The dynamic shift register is converted to a static latch by adding only one transistor. Thus the dynamic shift register (static latch) can be easily fabricated as part of a configurable logic element without adding significant complexity to the circuit or consuming significant semiconductor area. Because of the "hold" signal, the dynamic shift register can become a static latch because placing the shift register on hold automatically refreshes the data. Thus a separate refresh circuit is not needed.

It is apparent from the above description that the dynamic shift register (static latch) circuit does not need refreshing once it has been latched into a hold position. This is accomplished by use of the feedback circuit comprising lead 50-1 and pass transistor 54-1 in cell 5-1, for example.

Figure 7A shows an additional configurable logic array containing a plurality of configurable logic elements. In particular, configurable logic elements 70-1, 70-2, 70-4 and 70-5 are shown in their entirety while configurable logic elements 70-3, 70-6 and 70-7 through 70-9 are shown partially. In particular, the complete interconnections of these last five logical elements are not shown. The structure shown in Figure 7A is merely illustrative of the types of configurations and connections which can be implemented using the configurable logic array of this invention and does not depict an actual circuit configured to carry out an intended function.

As shown in Figure 7A, given leads in the general interconnect structure can be interconnected by various general interconnection junctions. The symbols representing the interconnect junctions shown in Figure 7A are illustrated in Figure 7B. In particular, while the schematics depicting various interconnect junctions are to some extent self-explanatory, the conventions used in

Figures 7B-1 through 7B-7 are further explained in Figures 8A through 8G.

Figure 8A is the schematic of a circuit for making a number of different interconnections between four leads coming together at a junction point: horizontal leads 90-1 and 90-4 and vertical leads 90-2 and 90-3. Thus, pass transistor 2, when activated into the conducting state, connects lead 90-3 to lead 90-1. Pass transistor 1, when conducting, connects lead 90-3 to lead 90-4. Pass transistor 4, when conducting, connects lead 90-4 to lead 90-2 and pass transistor 3, when conducting, connects lead 90-1 to lead 90-2. Pass transistors 5 and 6, when off, separate leads 90-4 from leads 90-1 and separate lead 90-2 from lead 90-3, respectively. Thus, should it be desired to connect vertical lead 90-2 to vertical lead 90-3, pass transistor 6 is activated. Likewise, should it he desired to connect horizontal lead 90-1 to horizontal lead 90-4, pass transistor 5 is activated. The terminology used to represent the possible connections between a plurality of leads can become quite complex. Thus, a simplified notation system as shown in Figures 8B to 8D has been adopted.

In Figure 8B, a plurality of pass transistors 92-1 through 92-13 are shown. The convention adopted in Figure 8B is to have a given pass transistor represented by a single short line. Thus, the line labelled 92-1 represents a pass transistor. Pass transitor 92-1 is drawn so that its two ends point to the ends of the leads 91-5 and 91-6 being interconnected by pass transistor 92-1. Similarly, the right end 93a of pass transistor 92-1 is aimed to the end 94a of lead 91-5. The left end 93b of pass transistor 92-1 is aimed to the end 94b of lead 91-6. For simplicity and to avoid cluttering the drawing in Figure 8B, the other ends of the transistors are not labelled. However, by visually aligning the line representing a given pass transistor with the ends of the leads 91-1 through 91-6 the particular two leads inter-

connected by that pass transistor can be determined. Thus, pass transistor 92-7 interconnects horizontal lead 91-4 with horizontal lead 91-1. Pass transistor 92-13 interconnects horizontal lead 91-4 with horizontal lead 91-2. Pass transistor 92-12 interconnects lead 91-3 with lead 91-5. Similar connections can be made between the other pass transistors and the other leads. The table in Figure 11 lists the pass transistor connecting lead A with lead B.

The above description assumes that only two leads are to be interconnected. If more than two leads are to be interconnected, the structure of Figure 8B can also be used for this purpose. Thus, lead 91-3 can be connected to lead 91-2 by turning on pass transistor 92-10. Simultaneously, lead 91-3 can be connected to lead 91-4 by turning on pass transistor 92-13. Alternatively, lead 91-3 could be connected to lead 91-4 by turning on pass transistor 92-11. Of course, this would also connect lead 91-4 through lead 91-3 and pass transistor 92-10 to lead 91-2. In addition, lead 91-6, for example, could be connected to the three leads 91-2, 91-3, 91-4 by turning on pass transistor 92-8. The number of interconnections which can be made using this structure is limited only by the imagination of the designer. In the limit, if all the pass transistors are turned on, all the leads 91-1 to 91-6 are interconnected. The resulting structure has a large capacitance which can actually be used in circuits as a component. Of course, all leads in Figure 8B can be interconnected by turning on as few as five leads. Note that in Figure 8B leads 91-1 and 91-2 cannot be directly connected to each other nor can lead 91-4 be directly connected to lead 91-5 without involving another lead. However, this ommission is not of importance because in general in an integrated circuit there is no need for two horizontal leads to carry the same signal. Of course, two additional pass transistors could be added to the structure of Figure 8B if Figure 8B is considered to be

merely a symbolic representation of intersecting leads and leads 91-1 and 91-2 are merely shown for convenience as being parallel but in fact represent non-parallel leads on an integrated circuit.

Turning to Figure 8C another possible interconnection topology is illustrated. In Figure 8C leads 1 to 8 are shown coming together at a complicated junction. Leads 1 and 8 are parallel horizontal to the left, leads 4 and 5 are parallel horizontal to the right, leads 2 and 3 are parallel vertical up and leads 6 and 7 are parallel vertical down. Looking for a moment at lead 6, the end 6a of lead 6 can be connected sensibly to the ends "a" of leads 1, 2, 3 , 4, 5 and 8. It is not sensible to connect lead 6 to lead 7 because theoretically the two leads are going in one direction only one lead is required to carry the necessary information in that direction. Since lead 6 has six desirable possible connections and each of the other seven leads also has 6 desirable possible connections there are a total of forty-eight desirable possible connections between the eight leads of Figure 8C. Since a given pass transistor connects two ends, twenty-four pass transistors are required to make the desired forty-eight connections. Each pass transistor has its ends labelled in Figure 8C to illustrate the leads which are connected by a given pass transistor. Thus, pass transistor 6-8 interconnects the end 6a of lead 6 to the end 8a of lead 8. Pass transistor 7-5 interconnects the end 7a of lead 7 to the end 5a of lead 5. Because of the complexity of the structure of Figure 8D a slightly different convention (a line with numbers on both ends) has been adopted for representing the pass transistor than was described above in conjunction with Figure 8B.

Figure 8D illustrates a configuration similar to that of Figure 8C with only twenty interconnection transistors rather than the twenty-four shown for the junction in Figure 8C. As shown in Figure 8D pass transistors

1-6, 7-4, 2-5 and 8-3 have been deleted from the transistors shown in Figure 8C.

Figure 8E illustrates the direct connections that would be possible if the four pass transistors omitted from Figure 8C were in fact included. (A connection between lead A and lead B is direct if A and B are connected by a single pass transistor.) The dashed lines show the direct interconnections possible by these omitted transistors. Figure 8D shows only twenty pass transistors whereas twenty-four pass transistors are necessary to make all possible direct connections. Figure 8F illustrates, however, the way in which it is possible to interconnect leads 4 and 7 without the four transistor connections shown in Figure 8E being present. Thus, for example, to connect lead 4 to lead 7, lead 4 is connected directly to lead 8 by means of transistor 4-8 while lead 8 is connected to lead 7 by pass transistor 8-7.

Note that each of the interconnections shown above in Figures 8A through 8E requires only one pass transistor in order to connect one junction lead to another junction lead while for the particular configuration illustrated in Figure 8F two pass transistors are required.

Figure 8G illustrates types of possible interconnections. The leads interconnected are illustrated by showing continuous stright line segments meeting. These interconnections are self-explanatory.

The symbology used in Figures 7B-1 through 7B-7 is identical to the symbology just explained in conjunction with Figures 8A through 8G. Thus, for example, Figure 7B-7 illustrates a solid block involving a twenty pass transistor junction. The twenty transistor interchange shown in Figure 7B-7 corresponds precisely to the interchange explained in more detail above in conjunction with Figure 8D.

Figure 7B-1 illustrates three transistors capable of making a T connection or a crossconnection but not a full interconnection. By full interconnection is meant the

ability to connect each of the leads (in Figure 7B-1, four leads) coming into a junction to any combination of other leads coming into the junction.

Figure 7B-2 shows a one transistor junction to connect a row with a column. Figure 7B-3 shows a six transistor full interconnection wherein any one of four leads coming into a junction can be connected to any one of the other three leads coming into the junction. Figure 7B-4 shows six leads coming into a junction wherein ten pass transistors are used to interconnect any one of the six input leads to any one of the five other leads of the junction. Figure 7B-5 illustrates a four-lead junction where two horizontal continuous leads are interconnected with two separate vertical leads using five pass transistors.

Figure 7B-6 illustrates a three-transistor junction wherein any one of three leads coming into a junction can be interconnected with any one of the other two leads. Figure 7B-7 illustrates the twenty-transistor junction for interconnecting any one of eight input leads to any one of the other eight input leads except that lead parallel and adjacent to the lead being interconnected as illustrated in Figure 8D and except for the four interconnections shown in Figure 8E (which also cannot be directly made using the structure of Figure 7B-7).

A CMOS transmission gate may be used in place of a pass transistor in implementing the interconnections described above.

Frequently, when interconnecting logic elements in a configurable logic array, such as the logic array shown in Figure 4A, which includes configurable logic elements 40-1 through 40-9, their input and output leads, their access junctions and the general interconnection leads and various general interconnect junctions, it is desired that the output signal from one configurable logic element be only connected to one or two other configurable logic elements. To facilitate interconnection, as a general

rule, it is desirable to position the one logic element as close as possible to the other logic element(s) to which it is to be connected.

Fig. 9 shows a portion of a configurable logic array, including configurable logic elements 9-1 through 9-6 and general interconnection leads L1 through L50, together with general interconnect junctions J1 through J12. The junction symbols in Figure 9 have the same meaning as explained in Figure 4b. One set of 30 access junctions is indicated by the dotted lines in Figure 9. This set includes 10 access junctions for the output leads of CLE 9-1 and 20 access junctions for the four input leads of CLE 9-2. The access junctions are not labeled individually for the sake of clarity. Referring to Figure 9, suppose, for example, that it is desired to connect a signal on output lead 1 of configurable logic element 9-3 to input lead 4 of configurable logic element 9-1, and that simultaneously it is desired to connect the output signal on output lead 1 of CLE 9-3 to input lead 1 of CLE 9-5. In order for the output signal on output lead 1 of CLE 9-3 to arrive at input lead 4 of CLE 9-1, it would be necessary for the signal to pass through at least four junctions, for example, access junction A10, general interconnect junction J4, general interconnection junction J1 and access junction A20. Similarly, in order to arrive at input lead 1 of CLE 9-5, it would be necessary for the signal on output lead 1 of CLE 9-3 to pass through at least four junctions. For example, access junction 10, general interconnect junction J10, general interconnection junction J7 and access junction A30. Similarly, if it is desired for the output signal on output lead 2 of CLE 9-3 to be connected to input lead 4 of CLE 9-4, it would be necessary for the signal to pass through at least two junctions and at least a portion P of the general interconnect lead L38 between these two junctions. For example, the output signal on lead 2 of CLE 9-3 might pass from output lead 2 via access junction A40 via the

marked portion P of general interconnect lead 39 to access junction 50 on input lead 4 of CLE 9-4. Thus, even though configurable logic element 9-3 has been positioned in the configurable logic array shown in Figure 9 so that it is next to configurable logic array 9-1, 9-5 and 9-4, it is nevertheless necessary for the output signals from CLE 9-3 to pass through several junctions and at least a portion of a general interconnect lead in order to arrive at the proper input lead. This utilization of the general interconnect leads is reduced in one embodiment of the invention by providing each CLE with a special vertical lead which enables one output lead of each configurable logic element to be directly connected to any input lead of the configurable logic element directly above it or below it in the configurable logic and by providing a special horizontal lead circuit which connects the second output of each CLE directly to a selected input lead of the CLE to its immediate right in the configurable logic array. For example, Figure 10 shows CLE 9-3 provided with a special vertical lead circuit (SVC) of the present invention which connects output lead 1 selectably to each input lead of CLE 9-1 and 9-5 directly above and below CLE 9-3. The SVC circuit includes lead S1 connected to output lead 1 and programmable access junctions P1, P2, P3, P4 for selectively connecting lead S1 with a desired input lead of CLE 9-1. The SVC also includes programmable access junctions P5, P6, P7 and P8 for selectively connecting lead S1 of CLE 9-3 with a desired input lead of CLE 9-5. Similarly, a special horizontal lead circuit (SHC) includes lead S2 connected to output lead 2 of CLE 9-3 and programmable access junctions P9, P10, P11, and P12 for selectivly connecting output lead 2 of CLE 9-3 with a desired input lead of CLE 9-4. The access junctions P1 through P12 are only indicated schematically in Figure 10, however, they each may be implemented by a single pass transistor and programmed in the manner described above for the junctions

of the general interconnect structures. The inclusion of such special interconnect circuitry has at least two advantages: first; it may reduce the overall usage of the general interconnect leads and junctions to the point where some of these leads and junctions may be eliminated from the configurable logic array. This, of course, depends on the interconnection demands of the other CLEs in the CLA. Secondly, the speed of the signals through these special interconnection circuits will be improved since the number of transmission gates or pass transistors and the amount of capacitance on the path will be reduced. Provision of special interconnection circuits is particularly useful when implementing MSI type functions, for example, shift registers and counters, where adjacent logic elements must be interconnected.

In view of the above description, which is illustrative only, it will be evident to one of ordinary skill in the art that a variety of special interconnections between adjacent configurable logic elements in a configurable logic array may be provided within the scope of the invention.

CLAIMS

1. A configurable logic array comprising:

a plurality of configurable logic elements (CLEs), each CLE having at least one input lead and at least one output lead;

a general interconnect structure comprising a plurality of general interconnect leads and a plurality of programmable general interconnect junctions for interconnecting selected ones of the general interconnect leads;

one or more access junctions for each input lead for connecting a corresponding general interconnect lead to said input lead;

one or more access junctions for each output lead for connecting the output lead to a corresponding general interconnect lead;

means for programming the general interconnect junctions and the access junctions such that there is an electrical path connecting a given output lead of a given CLE to a given input lead of a given CLE, the electrical path containing two access junctions and at least a portion of one of the general interconnect leads; and

at least one special interconnection circuit which permits a selected output lead of one of the CLEs to be connected to a selected input lead of another CLE, the special interconnection circuit not containing any portion of the leads or any junction in the general interconnect structure.

2. A configurable logic array as claimed in claim 1 comprising:

a first, a second, a third and a fourth CLE, the second CLE having a first output lead and a second output lead;

a first special interconnection circuit which permits an output signal on the first output lead

of the second CLE to be connected to a selected input lead of the first CLE and which also permits the first output signal to be connected to a selected input lead of the third; and

a second special interconnection circuit which permits an output signal on the second output lead of the second CLE to be connected to a selected input lead of the fourth CLE.

3. A configurable logic array as claimed in claim 1 or 2 wherein the special interconnection circuit comprises a lead connected to the selected output lead and a pass transistor for each input lead of the selected CLE connected between the lead connected to the selected output lead and the corresponding input lead.

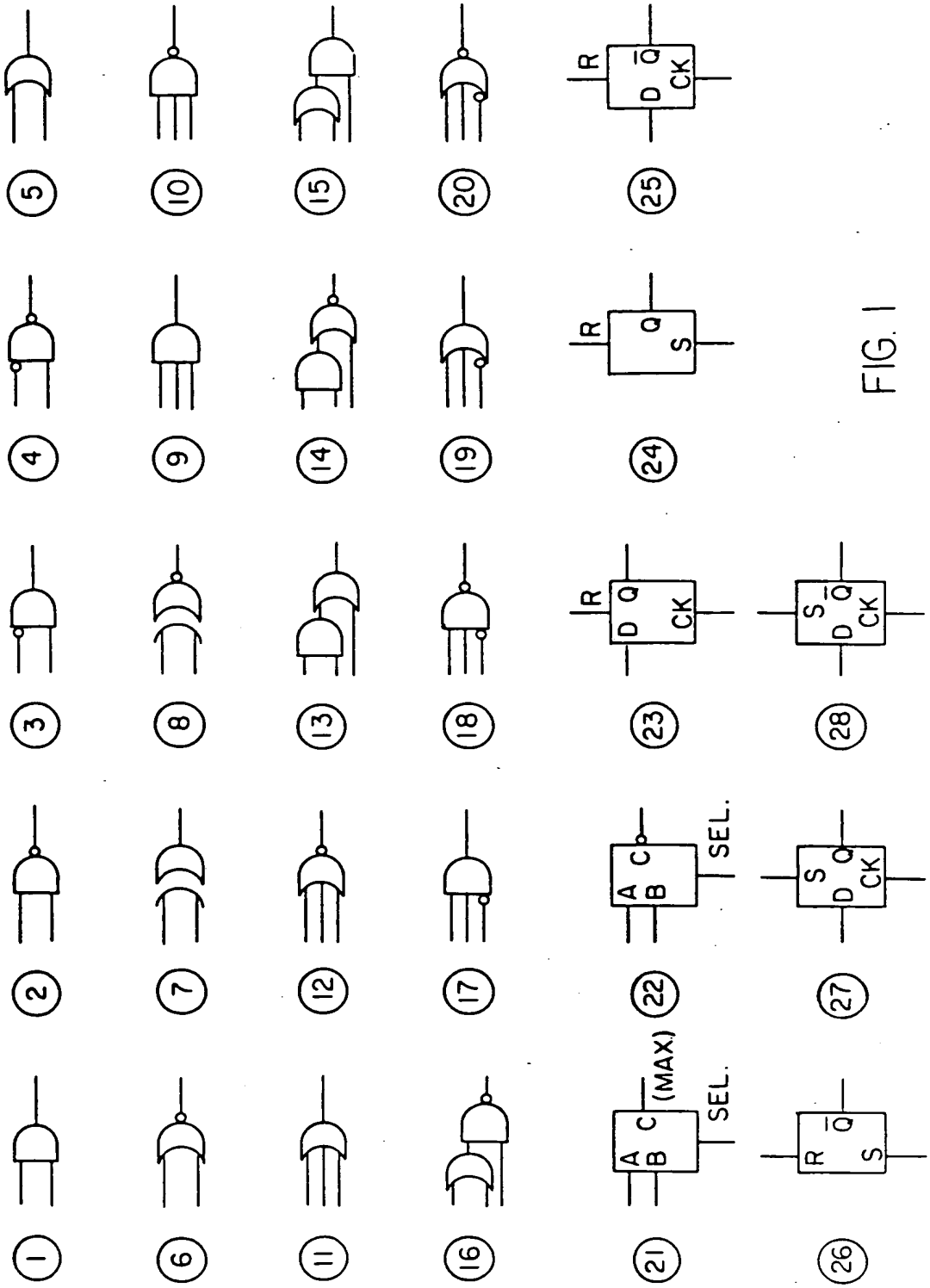

1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
A
B
C
(MAX)
SEL.
22
A
B
C
SEL.
23
R
D
Q
CK
24
R
S
Q
25
R
D
Q
CK
26
R
S
Q
27
S
D
Q
CK
28
S
D
Q
CK

FIG. 1

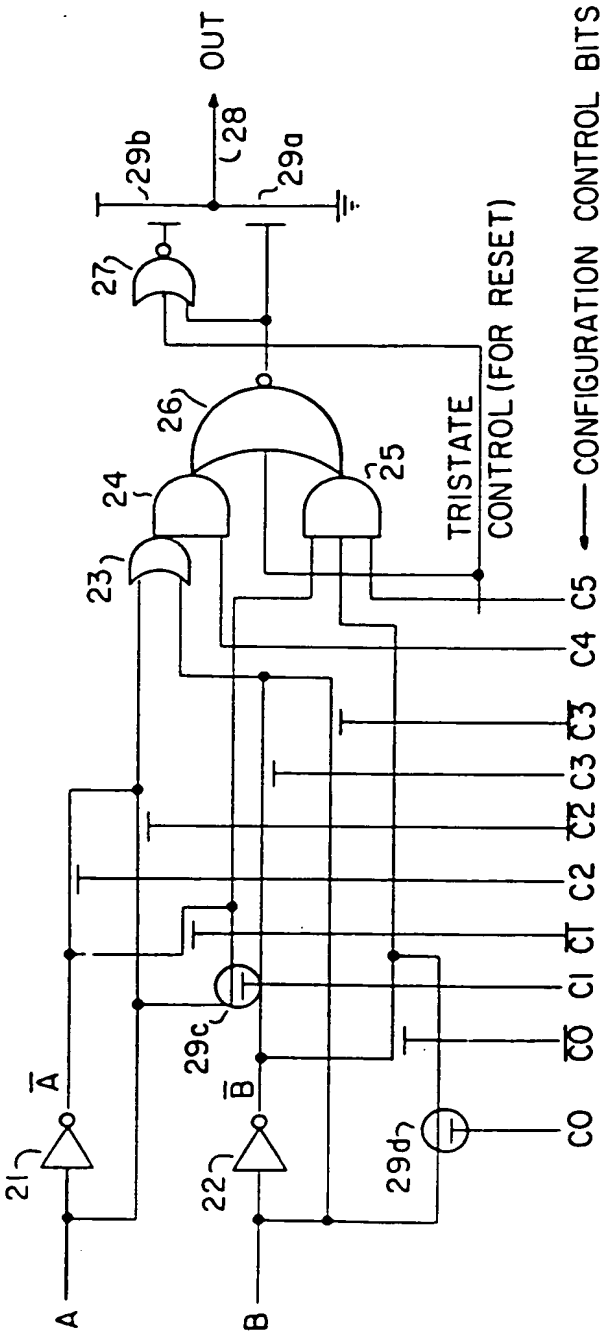


FIG. 2

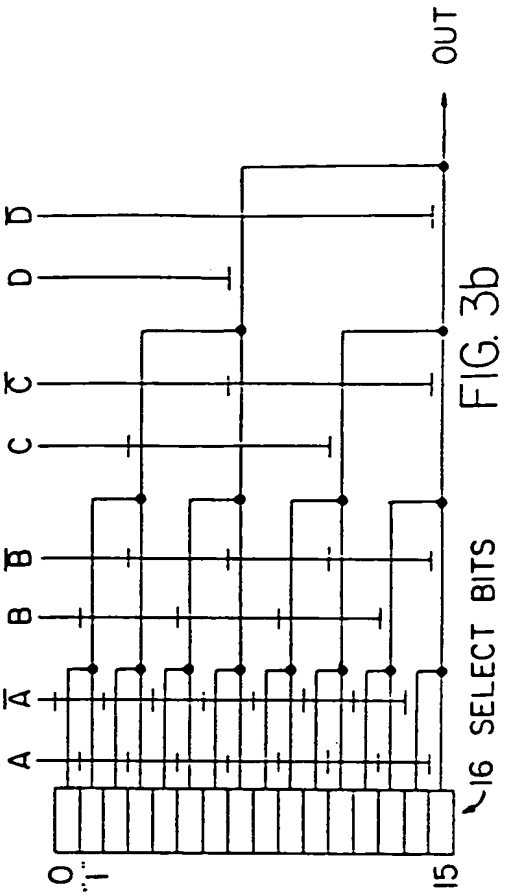


FIG. 3b

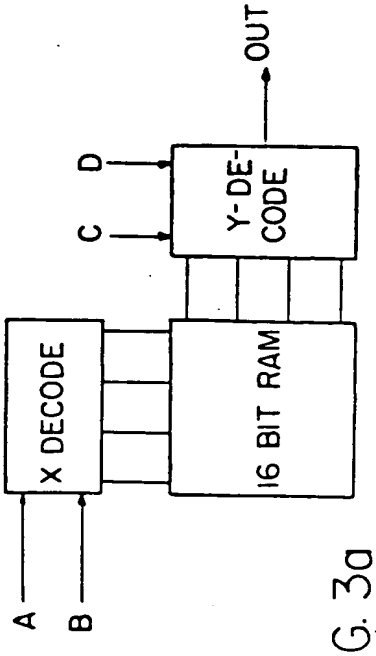


FIG. 3a

A B \ C D	0 0	0 1	1 1	1 0
0 0	1	0	0	0
1 0	0	0	0	0
1 1	0	0	0	0
0 1	0	0	0	0

FIG. 3c

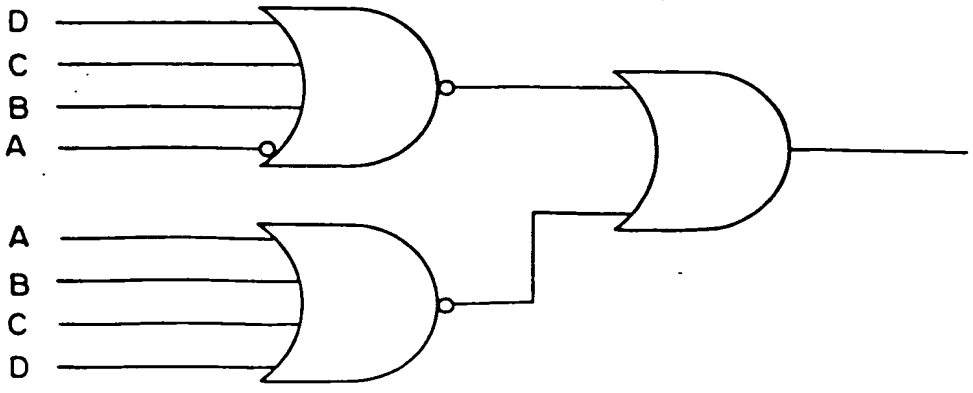


FIG. 3d

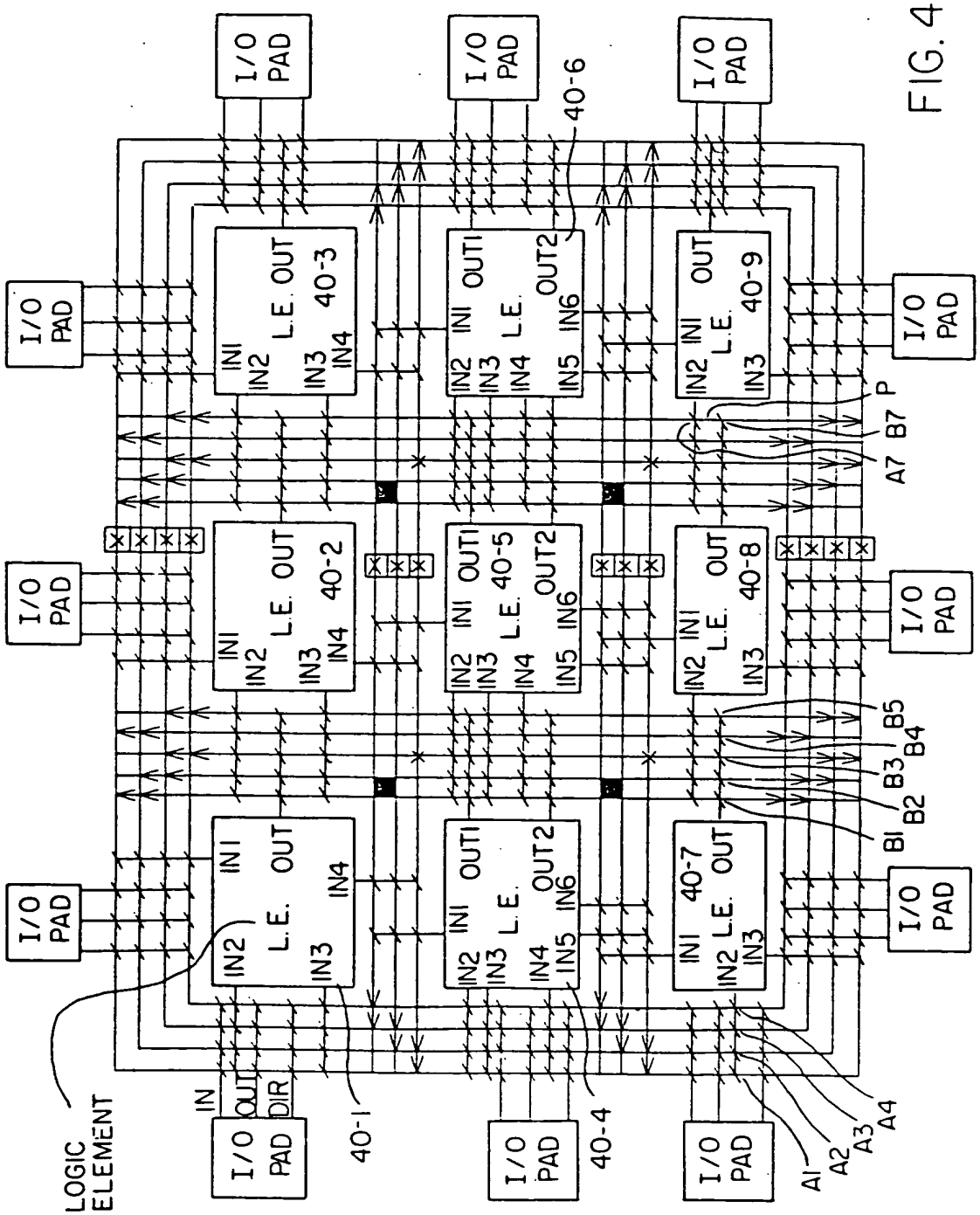
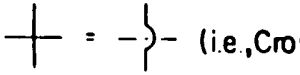

I/O PAD
L.E. OUT
IN1
IN2
IN3
IN4
IN5
IN6
OUT1
OUT2
40-1
40-2
40-3
40-4
40-5
40-6
40-7
40-8
40-9
LOGIC ELEMENT
IN
OUT
DIR
A1
A2
A3
A4
A7
B1
B2
B3
B4
B5
B7
P

FIG. 4a

 = (i.e., Crossover without Connection or Possibility of Connection)

 = or (i.e., Can Only be Connected or Disconnected, As Input or Output, But Cannot be Broken.)

 = Full Interchange - e.g. Figure 7B-7

 = Full Interchange - e.g. Figure 7B-3

 = Partial Interchange:  e.g. Fig. 7B-6

Lines (4 Vertical Shown) that do not have   Intersections are Intended to be Low Skew (i.e., Clock or Other) Paths.

 = Directional Amplifier (Direction is Selectable) to Prevent Signal Drooping Through too Many Pass Devices.

FIG 4b

0177261

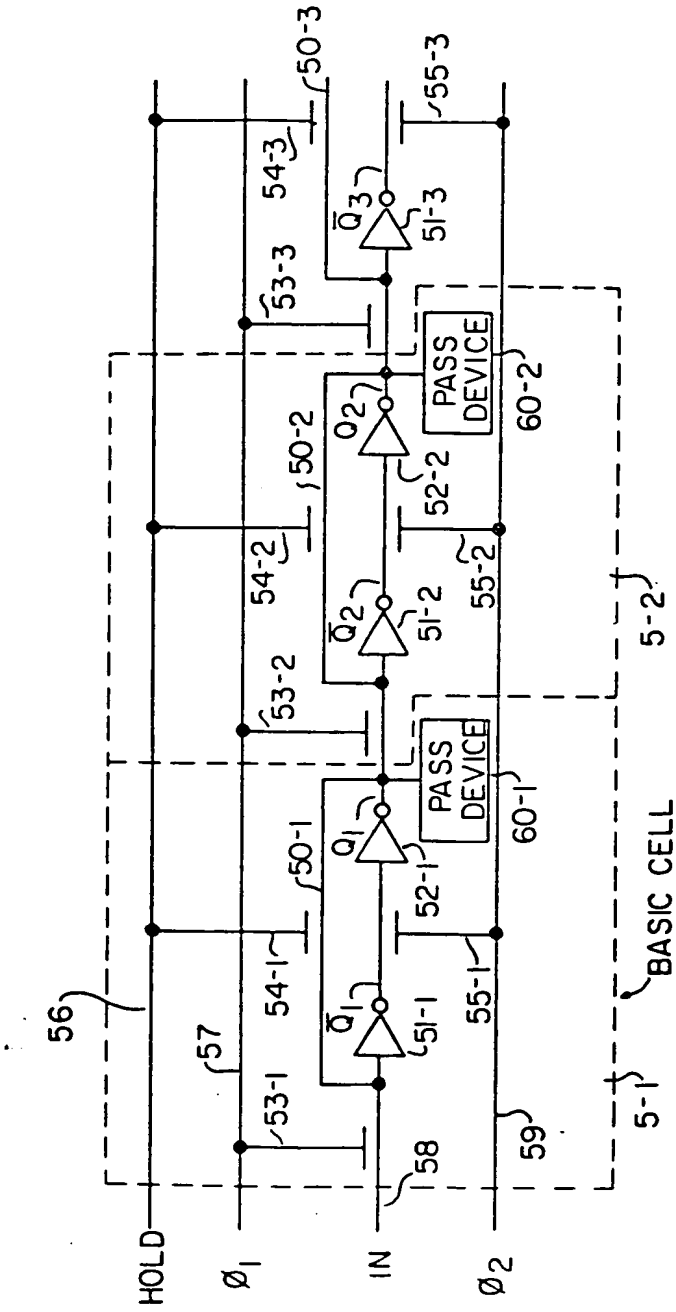

HOLD
Ø1
IN
Ø2
56
57
58
59
53-1
54-1
50-1
52-1
55-1
51-1
Q1
Q̄1
PASS DEVICE
60-1
53-2
54-2
50-2
52-2
55-2
51-2
Q2
Q̄2
PASS DEVICE
60-2
53-3
54-3
50-3
55-3
51-3
Q3
Q̄3
5-1
5-2
BASIC CELL

FIG. 5

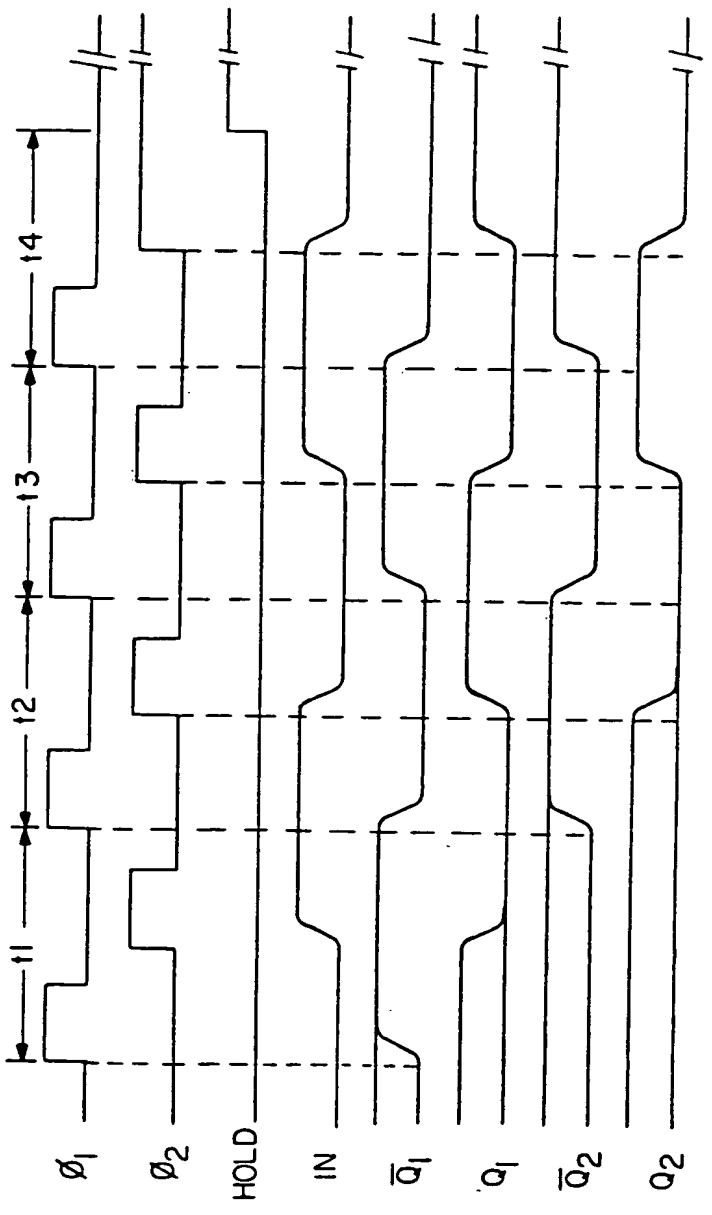


FIG 6a 6b 6c 6d 6e 6f 6g 6h

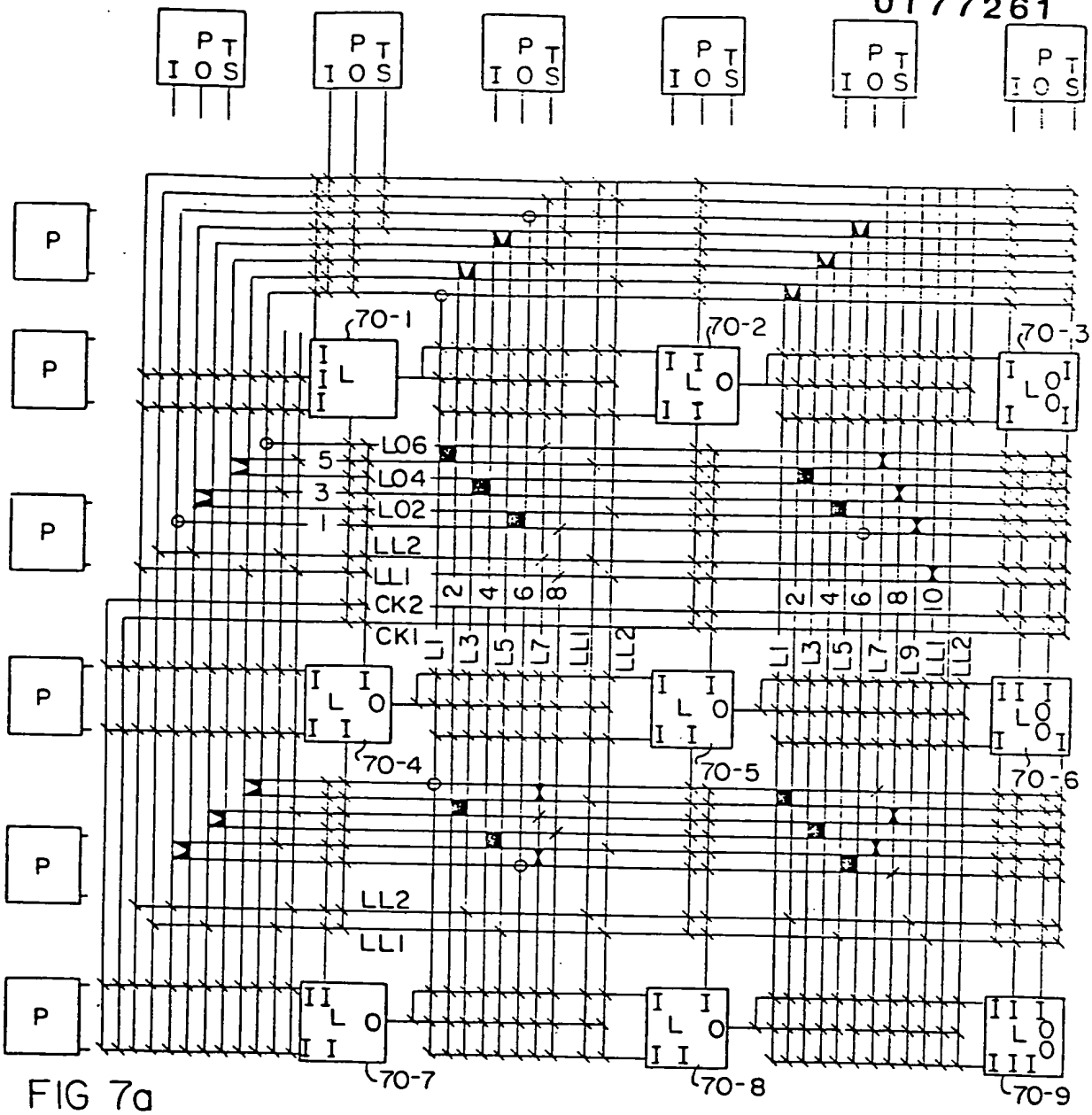
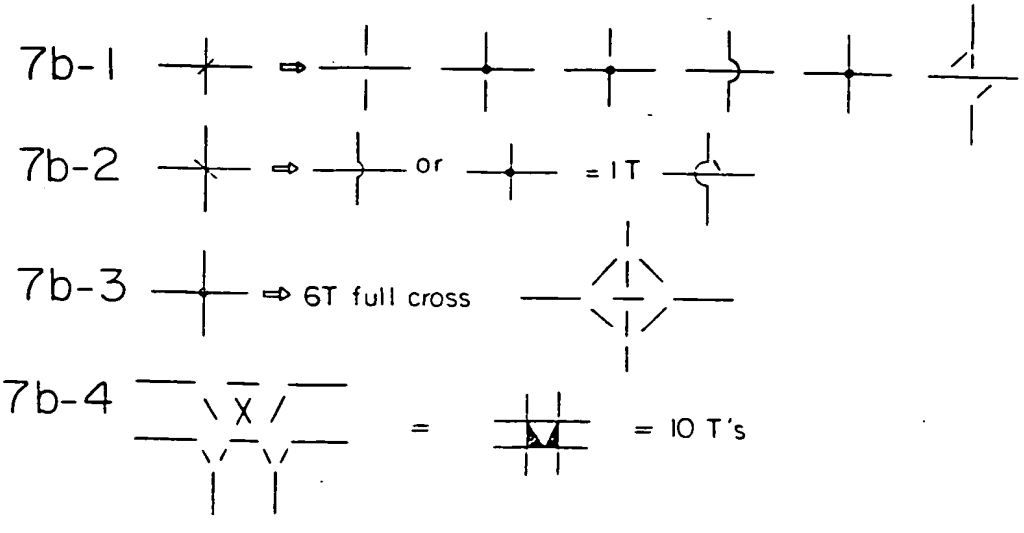
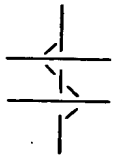

P T
I O S
P
70-1
70-2
70-3
70-4
70-5
70-6
70-7
70-8
70-9
L06
L04
L02
LL2
LL1
CK2
CK1
LL2
LL1

FIG 7a


7b-1
7b-2
or
= 1T
7b-3
6T full cross
7b-4
=
= 10 T's

7b-5  = 5 T's = 

7b-6  = 3 T's = 

20 T interchange

7b-7 

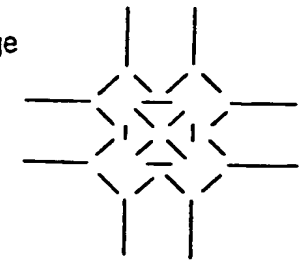


FIG. 7b

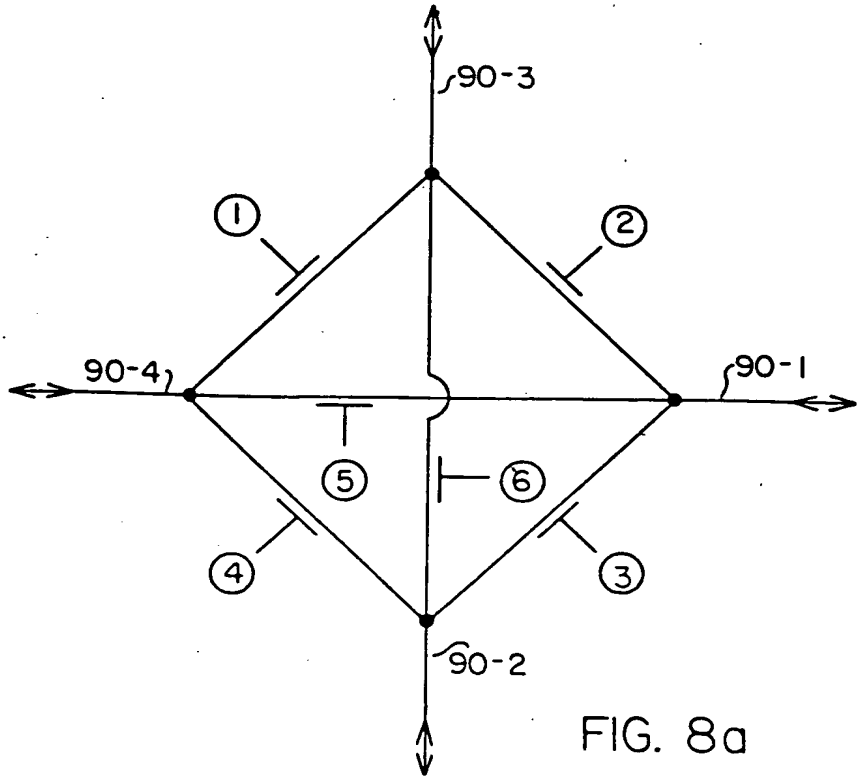


FIG. 8a

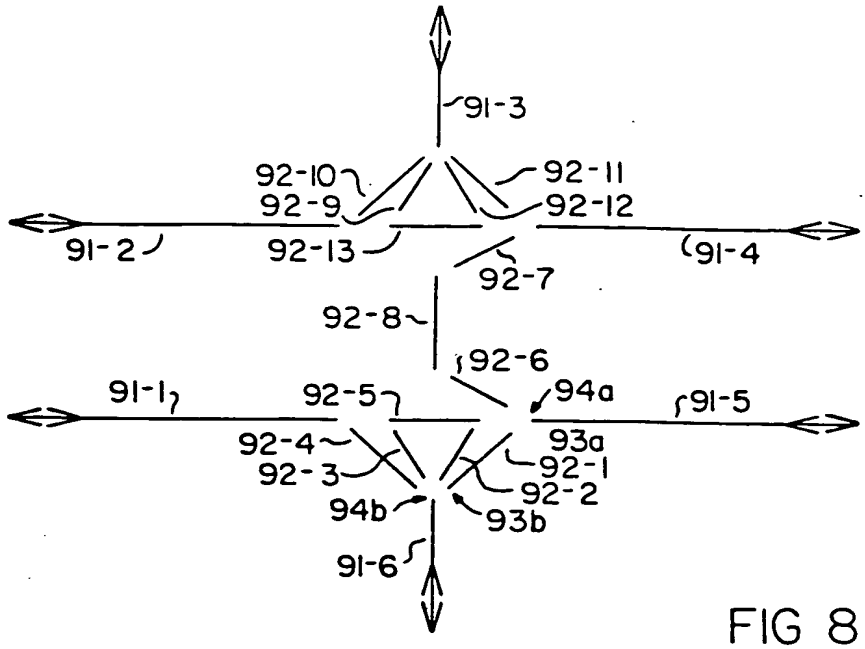

91-3
92-10
92-9
92-11
92-12
91-2
92-13
91-4
92-7
92-8
92-6
91-1
92-5
94a
91-5
92-4
93a
92-3
92-1
92-2
94b
93b
91-6

FIG 8b

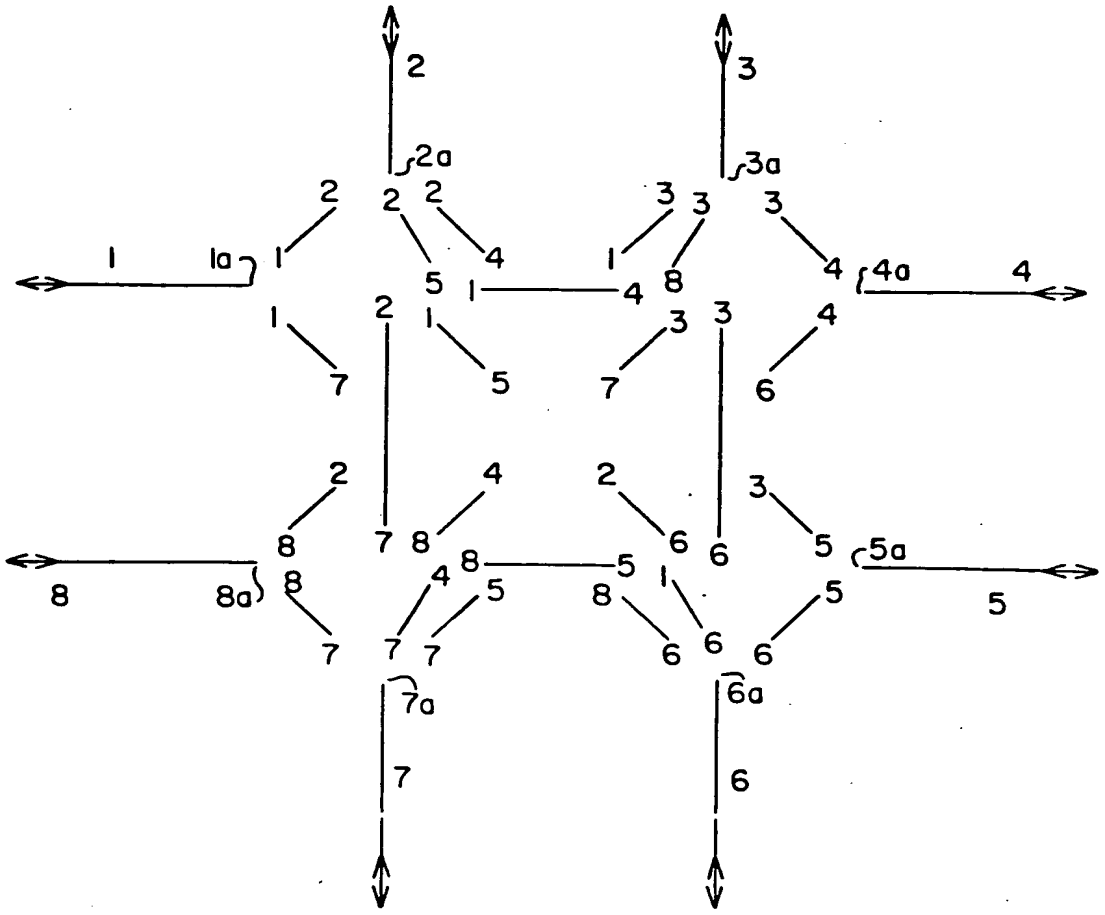

2
3
2a
3a
1
1a
4
4a
5
8
7
6
5a
8a
7a
6a

FIG. 8c

Circled numbers on ends of pass devices indicate which paths are directly connected.

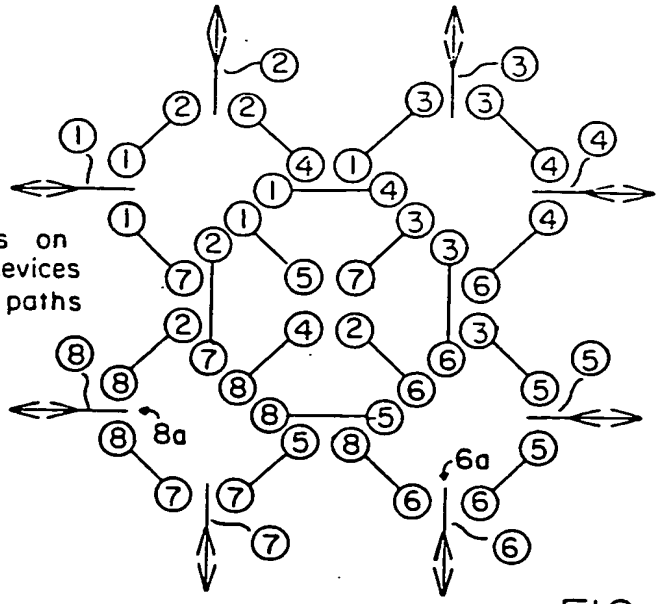


FIG. 8d

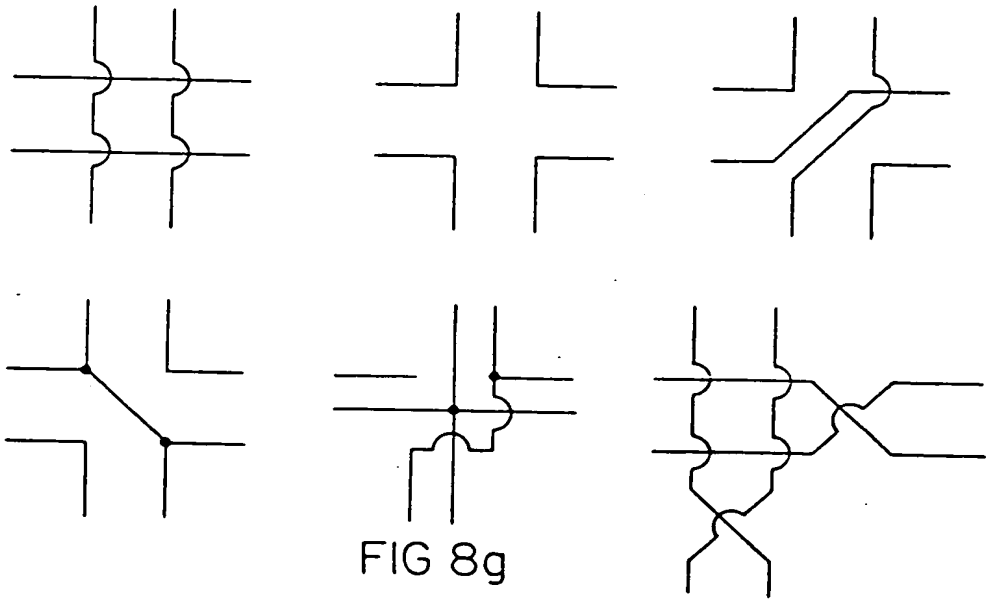
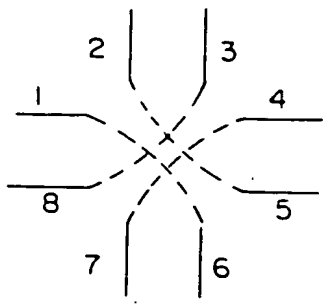
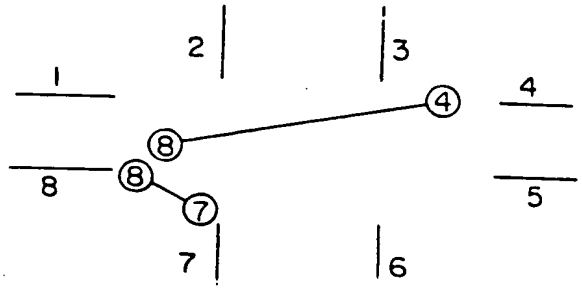
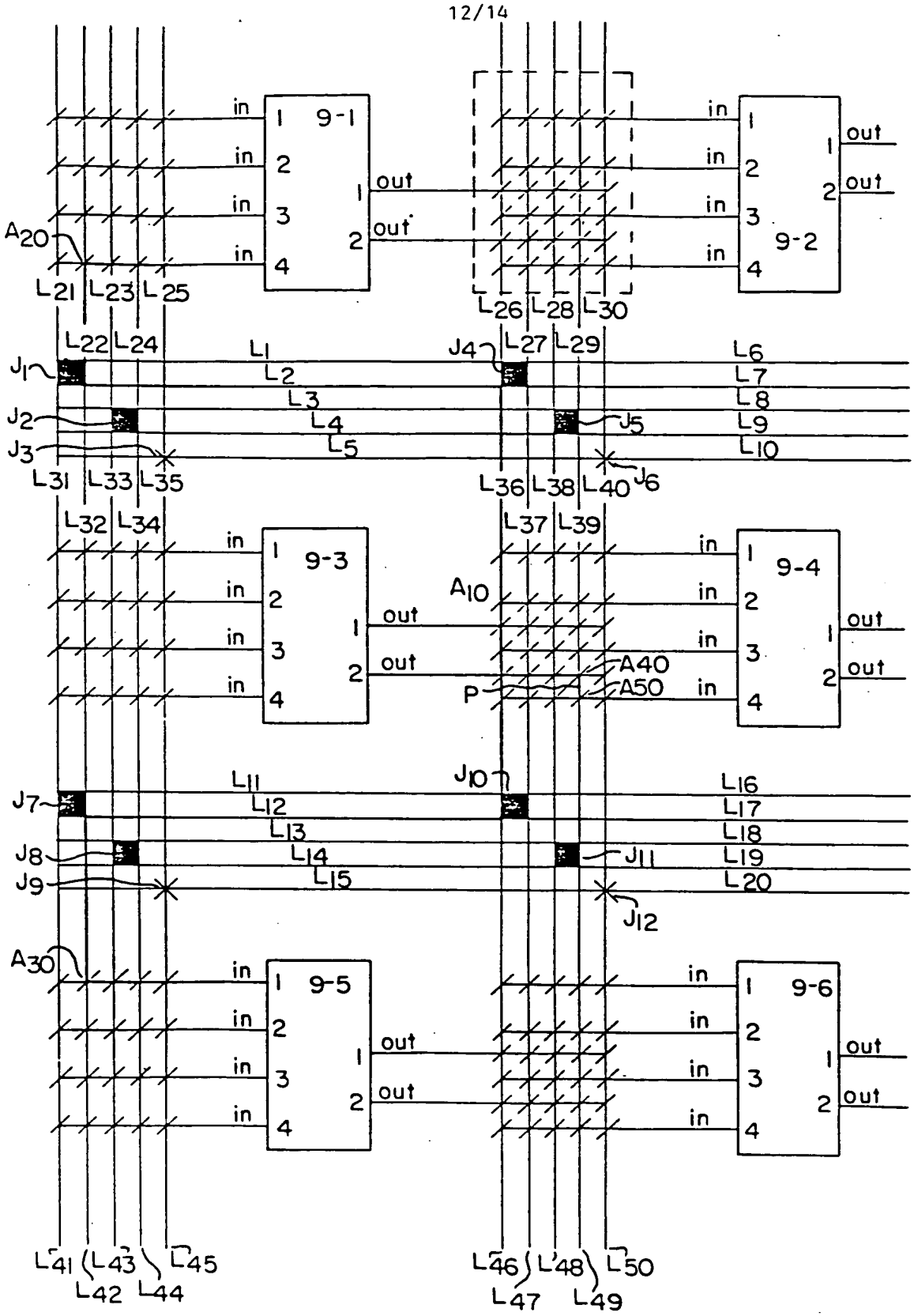


FIG 8g






9-1
9-2
9-3
9-4
9-5
9-6
in
out
A20
A10
A30
A40
A50
P
J1
J2
J3
J4
J5
J6
J7
J8
J9
J10
J11
J12
L1
L2
L3
L4
L5
L6
L7
L8
L9
L10
L11
L12
L13
L14
L15
L16
L17
L18
L19
L20
L21
L22
L23
L24
L25
L26
L27
L28
L29
L30
L31
L32
L33
L34
L35
L36
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L40
L41
L42
L43
L44
L45
L46
L47
L48
L49
L50

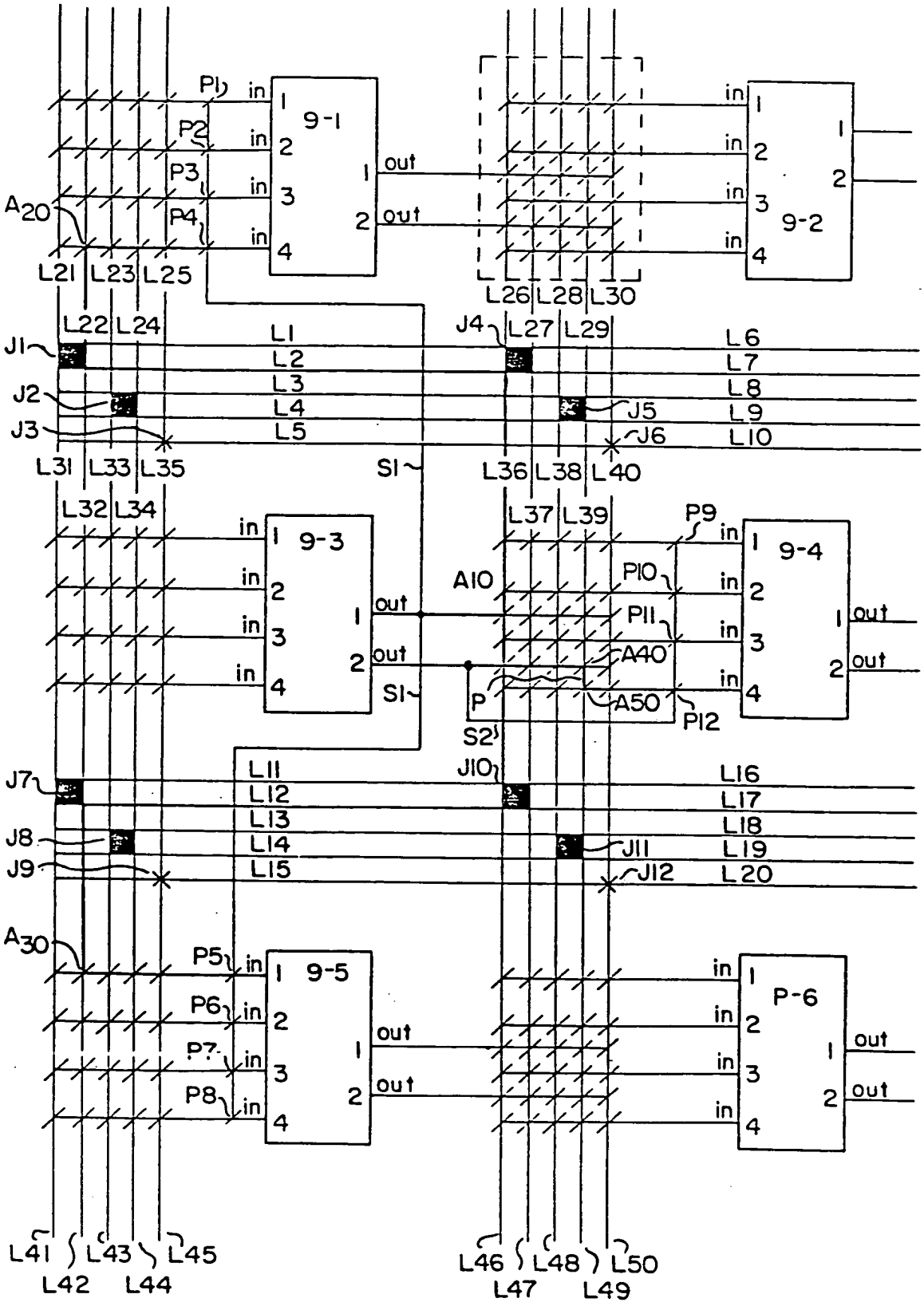
9-1
9-2
9-3
9-4
9-5
P-6
P1
P2
P3
P4
P5
P6
P7
P8
P9
P10
P11
P12
A20
A30
A10
A40
A50
P
S1
S2
J1
J2
J3
J4
J5
J6
J7
J8
J9
J10
J11
J12
L1
L2
L3
L4
L5
L6
L7
L8
L9
L10
L11
L12
L13
L14
L15
L16
L17
L18
L19
L20
L21
L22
L23
L24
L25
L26
L27
L28
L29
L30
L31
L32
L33
L34
L35
L36
L37
L38
L39
L40
L41
L42
L43
L44
L45
L46
L47
L48
L49
L50
in
out

FIG 10

LEAD A	PASS TRANSISTER	LEAD B
91-6	92-1	91-5
91-6	92-2	91-4
91-6	92-3	91-2
91-6	92-4	91-1
91-1	92-5	91-5
91-2	92-6	91-5
91-1	92-7	91-4
91-6	92-8	91-3
91-1	92-9	91-3
91-2	92-10	91-3
91-3	92-11	91-4
91-3	92-12	91-5
91-2	92-13	91-4

FIG.11

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